(51) International Patent Classification 5 :		(11) International Publication Number:	WO 94/09592
H04N 5/213	A1	(43) International Publication Date:	28 April 1994 (28.04.94)

(72) Inventors: TAKEMOTO, Sohei ; 35686 Conovan Lane, Fremont, CA 94536 (US). WOODHOUSE, Kenneth ; 265 Waverley, #1, Menlo Park, CA 94025 (US). GALLO, Luigi ; 800 Bear Gulch Road, Woodside, CA 94062 (US). STERN, John ; 2108 Monterey Avenue, Menlo Park, CA 94025 (US).

(54) Title: THREE DIMENSIONAL MEDIAN AND RECURSIVE FILTERING FOR VIDEO IMAGE ENHANCEMENT
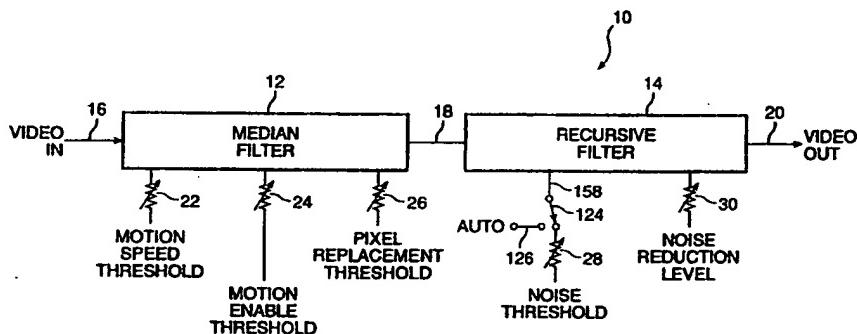
(57) Abstract

According to a presently preferred embodiment of the invention, image enhancement apparatus for digital video images comprises a two-stage filter (12) comprising a median filter (12) and recursive filter (14). The median filter operates in one, two, and three dimensions wherein the cluster of pixels framing the center pixel are ranked, and the median value of the pixel cluster is chosen as the correct pixel value. The pixel cluster configuration is selectable, as are the planes where the pixels are located. Multiple weights may be given to the appropriate median filter inputs. A motion detector (78) is used to prevent replacement of each pixel by its pixel cluster median value when there is excessive motion. Finally an adjustable pixel-replacement threshold is defined. Each pixel must deviate from its median value before it is replaced by that value. In the presence of rapid motion in the picture, the operation of the medial filter is reduced or halted by a properly derived motion signal according to the present invention, thus preventing motion artifacts from occurring.

<u>SPECIFICATION</u>

THREE-DIMENSIONAL MEDIAN AND RECURSIVE FILTERING
.FOR VIDEO IMAGE ENHANCEMENT

<u>BACKGROUND OF THE INVENTION</u>

1. <u>Field Of The Invention</u>

The present invention relates to video image enhancement. More particularly, the present invention relates to digital electronic noise-reduction techniques for high-quality video image improvement.

2. <u>The Prior Art</u>

It is known in the prior art to use median filters and temporal-recursive filters as effective methods for video image noise reduction. These two filtering methods may be used individually, or in combination, for better overall performance.

Median filtering is also known as rank-value filtering or rank-order filtering. By any name it is a well-known image-processing technique that combines pixels in a non-linear manner, and is particularly effective against impulsive noise and film grain and dirt when a three-dimensional pixel cluster is employed. Because median filters operate on discrete pixel values, the video must be in digitized form by nature.

Recursive filtering combines pixels spaced by exactly one video frame in an algebraic manner through controlled feedback, and is effective at reducing random noise by decreasing the temporal resolution in the noisy areas of the image while always preserving the horizontal and vertical resolution. Recursive filtering is not restricted to digital video images by nature, although providing an exact one-frame recursion delay is difficult by any other means. Median filtering coupled with recursive filtering gives better overall noise-reduction performance than either method when used independently.

The use of median and recursive filters for image processing has been reported in the literature. United States Patent No. 4,058,836 to Drewery et al, teaches noise reduction by

1   means of a recursive filter controlled by a motion detector.   G. Wischermann, "Median

2   Filtering of Video Signals - A Powerful Alternative", SMPTE Journal July 1991, discloses

3   the benefit of the use of median filters in video images. A. Christopher et al., "A VLSI

4   Median Filter for Impulse Noise Elimination in Composite or Component TV Signals", IEEE

5   Transactions on Consumer Electronics, Vol. 34, No. 1, Feb. 1988, discloses the use of a

6   pixel-replacement threshold to reduce median filter artifacts. United States Patent No.

7   4,928,258 to May, teaches the use of a median filter in two and three dimensions with

8   multiple weighted inputs, also known as multiple-input counting. British Patent

9   Application No. GB 2 139 039 A to Storey, teaches electrical means for detecting the

10 presence of film dirt in video signals.

11   In addition, at least one commercially available noise reduction system employs both

12 median and recursive filtering. Broadcast Television Systems, Inc. of Salt Lake City Utah

13 offers a model MNR9 Median noise reducer which employs selectable pixel clustering. The

14 BTS product is prone to strong motion artifacts.

15   The state of the art in video image improvement using either median filtering or

16 recursive filtering falls short of providing sufficient performance, closely related to noise

17 reduction effectiveness, with acceptable motion artifacts and resolution loss in pictures

18 with high motion content. In order of discovery, the Drewery teaching of recursive-only

19 noise reduction is very fundamental, but the system performance reaches its limit for

20 images with average signal-to-noise ratio (SNR) before producing noticeable motion

21 artifacts. The concept of video random and impulsive noise reduction by means of a median

22 filter is shown by Wischermann. While in this application the performance is quite good

23 with still pictures, small motion in the picture produces motion artifacts and loss of video

24 resolution. Christopher et al. implemented a manual pixel-replacement threshold logic at

25 the output of a two-dimensional median filter in an attempt to minimize the blurring

26 artifacts, but use of this threshold alone compromises the median filter effectiveness. May's

27 invention is not geared toward high-quality video images, hence motion artifacts and

1   picture resolution loss are more acc ptable in his application. The Storey disclosur

2   represents the state of the art in motion detection, although there is no suggestion to employ

3   it in combination with a median filter.

4   It is an object of the invention to provide an apparatus and method for improving

5   digital video images by removing noise and film grain and dirt through the use of digital

6   electronic filtering, while creating a minimum of filtering artifacts.

7

8   BRIEF DESCRIPTION OF THE INVENTION

9   According to a presently preferred embodiment of the invention, image enhancement

10   apparatus for digital video images comprises a two-stage filter. The first stage of image

11   improvement consists of a median filter selectively operable in one, two, and three

12   dimensions (horizontal, vertical, and temporal, respectively) wherein the cluster of pix Is

13   framing the center pixel are ranked, and the median value of the pixel cluster is chosen as

14   the correct pixel value. In absence of video image motion, this process is very effective in

15   locating the most likely pixel value that belongs in the center of the cluster even in presence

16   of noise.

17   According to the present invention, the pixel cluster configuration of the median

18   filter is selectable, as are the planes where the pixels are located. Multiple weights may be

19   given to the appropriate median filter inputs. A motion detector is used to prevent

20   replacement of each pixel by its pixel cluster median value when there is excessive motion.

21   In addition, an adjustable pixel-replacement threshold is defined, and each pixel must

22   deviate from its median value by a threshold amount before it is replaced by that value. In

23   the presence of rapid motion in the picture, motion artifacts are readily generated in prior-

24   art median filter based systems because the median filter is unable to locate the correct

25   pixel value. The picture is thereby rendered unnatural. According to the present invention,

26   the operation of the median filter is reduced or halted by a properly derived motion signal

27   according to the present invention, thus preventing motion artifacts from occurring.

1   The second stage of image improvement makes use of the conventional recursiv

2   filter as taught by Drewery, operating in the time domain. This process is particularly

3   effective in averaging co-sited pixels temporally spaced and its effectiveness is enhanced

4   when preceded by a stage containing the median filter.

5   In the case of video signals obtained from film by a telecine, the invention is

6   particularly useful in removing film grain scratches and dirt as well as noise in the video.

7   The same embodiment is also most effective in handling very noisy video images containing

8   impulsive noise. The high level of video quality improvement is made possible by the use of

9   three-dimensional median and recursive filters operating in tandem. Both median and

10   recursive filters are optimally controlled through the use of motion detectors whose

11   threshold settings are coupled to the main control of noise reduction to maximize the level of

12   image improvement and minimize motion artifacts.

13   By cascading two stages of independently operating noise-reduction circuits utilizing

14   different principles of noise reduction with the aid of motion-detection processing and

15   control, it is possible to obtain the best results of noise reduction, impulsive noise

16   elimination, film grain reduction, removal or reduction of film dirt and scratches and

17   stabilization of picture jerkiness with a minimum of motion artifacts and loss of video

18   resolution.

19

20   BRIEF DESCRIPTION OF THE DRAWINGS

21   FIG. 1 is a block diagram of a presently preferred embodiment of a digital image

22   improvement system according to the present invention.

23   FIG. 2 is a block diagram of the computation core of the median filter of the digital

24   image improvement system of the present invention.

25   FIGS. 3a-3o are representations of various preferred median-filter cluster

26   configurations according to the present invention.

27   FIG. 4 is a block diagram of a median-filter motion processor for use in the digital

1   image improvement system of FIG. 1.

2   FIG. 5 is a block diagram of a presently preferred embodiment of the selector circuit

3   of FIG. 2.

4   FIG. 6 is a block diagram of a recursive filter for use in a presently preferred

5   embodiment of the present invention.

6   FIG. 7 is a diagram illustrating a preferred transfer function for the non-linear

7   transfer block of the recursive filter of the present invention.

8

9   DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

10   Those of ordinary skill in the art will realize that the following description of the

11   present invention is illustrative only and not in any way limiting. Other embodiments of the

12   invention will readily suggest themselves to such skilled persons.

13   Referring first to FIG. 1, a block diagram of a presently preferred embodiment of a

14   digital image improvement system 10 according to the present invention is presented. The

15   digital image improvement system 10 of the present invention comprises two main

16   subcomponents, median filter 12 and recursive filter 14. According to the present

17   invention, these two subcomponents are arranged in a cascade configuration. Thus a video

18   input bus 16 presents a stream of video pixels in real time to median filter 12. the output

19   of median filter 12 is presented as a stream of video pixels in real time on bus 18 to

20   recursive filter 14, and the output of recursive filter 14 on bus 20 comprises the output of

21   digital image improvement system 10.

22   As may be seen from FIG. 1, median filter 12 has user-selectable motion speed

23   threshold control 22, motion enable threshold control 24, and pixel replacement threshold

24   control 26. Recursive filter 14 has user-selectable noise threshold control 28 and noise

25   reduction level control 30. These controls will be more fully explained herein with respect

26   to median filter 12 and recursive filter 14.

27   Referring now to FIG. 2, median filter 12 is shown in more detail and is seen to

1   incorporate novel features which give it additional functionality representing an

2   improvement over the prior art.

3   Median filter 12 takes a multibit digital video signal from input bus 16 and passes it

4   through delay elements 32, 34, 36, and 38. Delay elements 32 and 38 delay the video

5   pixels by one frame minus one horizontal line, such that, at any given time, the pixel

6   present at their outputs are from the same horizontal position one line above the pixel

7   present at their inputs, but from the previous frame.   Delay elements 34 and 36 each delay

8   the video signal one horizontal line such that the pixel present at their outputs at any given

9   time is from the same horizontal position one line above the pixel present at their inputs

10   from the same frame. As will be appreciated by those of ordinary skill in the art, delay

11   elements 32, 34, 36, and 38 may comprise conventional digital delay elements, such as

12   serial shift register chains or the like.

13   The overall effects of delay elements 32, 34, 36, and 38 are such that if the current

14   pixel of interest is present at node 40 at the output of delay element 34, the pixels present

15   at nodes 42 and 44, the outputs of delay elements 32 and 36, respectively, will be the

16   pixels from the same horizontal positions in the lines immediately below and above the pixel

17   of interest. Further, the pixels present at nodes 46 and 48,the input of delay element 32,

18   will be the pixels from the succeeding and preceding frames, respectively, occupying the

19   same position in the those frames as the pixel of interest.

20   The heart of median filter 12 is rank-value filter element 50, which, according to a

21   presently preferred embodiment of the invention, may be a L64220 rank-value filter

22   integrated circuit, available from LSI Logic Corp., of Milpitas, California. The data sheet

23   for the L64220 rank-filter integrated circuit is expressly incorporated by reference

24   herein.   Rank-value filter element 50 includes a rank-selector circuit portion 52 which

25   takes inputs from a plurality of shift registers 54, 56, 58, 60, 62, 64, 66, and 68.   The

26   function of rank-selector circuit 52 is to select the median value from among the inputs

27   presented.

1   Shift registers 54, 56, 58, 60, 62, 64, 66, and 68 are eight-bit serial shift

2   registers in the L64220 integrated circuit, but those of ordinary skill in the art will

3   recognize that other configurations are possible.   By employing these serial shift registers,

4   the present invention can define the median value of the pixel of interest in terms of the

5   pixels to its immediate left and right, as well as pixels immediately above and below (from

6   delay elements 34 and 36).

7   Rank-value filter element 52 is controlled by control unit 70, which selects which

8   pixel values stored in the shift registers 54, 56, 58, 60, 62, 64, 66, and 68 are used in

9   the median value determination. As disclosed in the L64220 Data Sheet from LSI Logic,

10   expressly incorporated by reference herein, any pixel element in the shift registers 54,

11   56, 58, 60, 62, 64, 66, and 68 can be masked such that the pixel cluster used to compute

12   the median value is selectable.   Loading of the masking registers in the L64220 integrated

13   circuit is easily and routinely accomplished by employing the address, clock, and write-

14   enable inputs provided.   Those of ordinary skill in the art will recognize that a

15   microcontroller could easily be employed to provide selectable clusters by controlling the

16   address, clock, and write-enable inputs to load preselected patterns into the mask registers

17   in the control section 70 of rank-value filter element 50.

18   From an examination of FIG. 2, those of ordinary skill in the art will readily

19   recognize that the pixels from nodes 40, 46, and 48 are each presented to two shift

20   registers at the same time. Thus, the pixels present at node 46 are presented to shift

21   registers 54 and 56, the pixels present at node 40 are presented to shift registers 60 and

22   62, and the pixels present at node 48 are presented to shift registers 66 and 68. This

23   arrangement allows the possibility of double-counting these pixel values in the median

24   value computation.

25   Referring now to FIGS. 3a-3o, diagrammatic representations of the various pixel

26   clusters from which the median value can be calculated are shown according to a presently

27   preferred embodiment of the invention. FIGS. 3a-3o show combinations of both positional

1   and temporal clustering, using left, right, horizonal, vertical, and diagonal nearest

2   neighbors in the positional domain, and corresponding past and next frame pixels and their

3   immediate left, right, horizonal, and vertical neighbors in the temporal domain. From FIGS.

4   3a-3o, those of ordinary skill in the art can see the cluster geometries made possible by use

5   of the delay elements 32, 34, 36, and 38. Each pixel position is represented by a circle and

6   the double-counted pixels are shown as double circles. The present embodiment can accept

7   any pixel cluster covering the present frame with 0, 1 or 2 votes, the preceding and

8   following frames both with 0, 1 or 2 votes, and the lines above and below each with 0 or 1

9   votes. According to the presently preferred embodiment of the invention, only the

10   corresponding pixels in the immediately preceding and succeeding frames may be double-

11   counted by having 2 votes, since these pixels introduce the least degradation of spatial

12   resolution, but those of ordinary skill in the art will realize that other configurations are

13   possible by suitably modifying the delay elements and doubling of serial shift register

14   inputs. Each cluster configuration except for that illustrated in FIG. 3o is symmetric in

15   each of the 3 dimensions. The configuration FIG. 3o may be used when the median filter is

16   inactive, and a minimum overall video delay is desirable. The selection of which pixel

17   cluster to employ may be user-selectable by means of, for example, a simple selector

18   switch.

19   Referring again to FIG. 2, a compensation delay 72 is connected to node 40 in order

20   to enable complete bypassing of median filter 12. The amount of delay provided by

21   compensation delay 72 is such as to provide at its output the pixel value whose computed

22   median value is simultaneously present at output 74 of rank-value filter 50. The output of

23   compensation delay 72 and the output 74 of rank-value filter 50 are provided to selector

24   76. The function of selector 76 is to pass the pixel value from one of compensation delay 72

25   and the output 74 of rank-value filter 50 to output bus in response to a threshold select

26   signal. The structure and operation of selector 76 will be described with reference to FIG.

27   5.

1   A motion detector circuit 78 is advantageously employed in m dian filter 12 to

2   reduce the amount of temporal filtering so as not to introduce blurring motion artifacts in

3   moving areas of the image which require full temporal resolution. The structure and

4   operation of a presently preferred motion detector 78 will be described with reference to

5   FIG. 4, to which attention is now drawn.

6   Referring now to FIG. 4 , it may be seen that motion detector 78 comprises two

7   sections, motion processor 80 and global motion detector 82, both shown within dashed

8   lines on FIG. 4. Motion processor 78 operates on the luminance portion of the digital video

9   signal and two signals delayed by one frame each using frame delays 84 and 86, which may

10   comprise conventional digital delay elements. As indicated on FIG. 4, the output of frame

11   delay 86 is a pixel from frame A, the output of frame delay 84 is the corresponding pixel

12   from frame B, and the input to frame delay 84 is the corresponding pixel from frame C,

13   where frame B is a current video frame and frames A and C are the proceeding frame and the

14   following frame. Where there are differences in the pixel values of the corresponding pixel

15   in frames A, B, and C, these differences could be caused by motion in the picture or, for

16   images originated from film, from dirt and or scratches on the film. It is therefore

17   imperative to derive motion information from the video itself if the frame contains

18   interframe motion, in order to prevent erroneous operation of the median filter which will

19   smear the image by misinterpreting motion as noise or dirt.

20   Motion processor 80 derives three signals, IA-BI, IB-CI, and IA-CI, using digital

21   subtractor circuits 88, 90, and 92, and absolute value circuits 94, 96, and 98, which may

22   comprise ROM look-up tables, as is known in the art. The Global Motion Detector 82

23   operates by processing the absolute frame difference IB-CI from absolute value circuit 96.

24   The IB-CI difference is processed through a line integrator circuit 100, comprising an

25   accumulator active each pixel and reset each line, latch 102, line average circuit 104

26   which may comprise an accumulator active each line and reset each field, and minimum

27   detect circuit 106, which may comprise a digital comparator active each line and reset each

9

1   field to compare the latest line integration value with the minimum line integration value,

2   to determine the floor of video activity of every active video line, and the average value of

3   motion through a frame by the Line Average circuit. The higher the motion content in the

4   frame, the larger is the output of the line average circuit 104.

5   At the end of the video frame, the minimum detect and line average values are

6   subtracted in subtractor circuit 108, and the difference is latched at each field time in latch

7   110. The Value stored in latch 110 is compared with a threshold value supplied on motion-

8   speed threshold line 24 in decision logic 112 to determine if the frame is considered to

9   contain fast motion or slow motion. According to a presently preferred embodiment of the

10   invention, the threshold value is user-selectable, for example, under computer control as is

11   well known in the art. The fast-motion/slow-motion determination at the output of decision

12   logic 112 is a binary on/off decision.

13   In the Motion Processor block, three interframe comparisons of temporally co-sited

14   pixels, IA-BI, IB-CI, and IA-CI are made in subtractor circuits 88, 90, and 92 and absolute

15   value circuits 94, 96, and 98. According to a presently preferred embodiment of the

16   invention, it has been determined that the larger of the first two comparison levels is the

17   better representation of motion for fast-moving motion content. This selection is made by

18   larger-value select circuit 114, which may comprise a digital-word comparator. For

19   slow-moving images, the IA-CI comparison is best. Data select circuit 116, which may

20   comprise a digital multiplexer, is used to select the output representing fast or slow motion

21   depending on the output of decision logic 112.

22   The most suitable motion signal selected by data select circuit 116 is subsequently

23   filtered in two dimensions (horizontally and vertically) by 2D filter circuit 118 to enhance

24   the signal-to-noise ratio of the motion signal. 2D filter circuit 118 may preferably

25   comprise a horizontal filter of seven points and a vertical filter of three points, although

26   other configurations are possible. If the selected and filtered signal is above the motion-

27   enable threshold 24, decision logic 120 will disable the operation of the median filter in a

10

1   binary on/off fashion at its enable input 122 (FIG. 2). The threshold setting of decision

2   logic circuit 120 is user-adjustable by loading a selected threshold value into a register

3   inside decision logic circuit 120, for example, under computer control as is well known in

4   the art.

5   Pixel-replacement Threshold Logic selector 76 (FIG. 2) compares the median filter

6   output to the corresponding pixel at the center of the pixel cluster and, if the difference is

7   above the threshold value 26 set by the user, the median value is selected. Referring now to

8   FIG. 5, the structure and operation of selector 76 will be described. The comparison of the

9   median filter output and the central pixel value is made in subtractor circuit 150 and

10   absolute-value circuit 152. Decision logic 154, which may comprise a digital-word

11   comparator, decides if the compared value exceeds pixel replacement threshold 26 and

12   issues a binary on/off output in response. Data selector circuit 156, which may comprise a

13   multiplexer, selects either the computed median or the central pixel value for ultimate

14   median filter output. The threshold settings for decision logic 152 are adjustable by user

15   control, for example, under computer control as is well known in the art.

16   FIG. 6 is a block diagram of recursive filter 14 according to a presently preferred

17   embodiment of the invention. The operation of recursive filter 14 is controlled by the noise

18   threshold adjustment 28 and by the noise reduction level, adjustment 30, in the Manual

19   Threshold mode. According to a presently preferred embodiment of the invention,

20   recursive filter 14 may be a filter such as the one set forth in United States Patent No.

21   4,058,836, expressly incorporated herein by reference.

22   According to a presently preferred embodiment of the invention, an automatic mode

23   of operation of recursive filter 14 is provided wherein the noise threshold adjustment is

24   replaced by the Global Motion Detector level, updated every frame instant. This is

25   illustrated symbolically by switch 124, which is switchable to an automatic operating node

26   comprising the output of global motion detector 82 at automatic node 126. Switch 124 thus

27   provides either a manual user-adjustable nois threshold control or an automatically

11

1   determined noise threshold control at point 158. FIG. 6 is a block diagram illustrating a

2   recursive filter similar to the one disclosed in United States Patent No. 4,058,836. Vid o

3   input is provided to one input of subtraction circuit 160. The output of subtraction circuit

4   160 is presented to the input of low pass filter 162, which is configured to smooth the

5   difference signal as disclosed in United States Patent No. 4,058,836. The output of

6   subtractor 160 is also presented to compensating delay 164, which compensates for the

7   delay through low pass filter 162. The output of compensating delay 164 is presented to one

8   input of multiplier 166. The other input of multiplier 166 is supplied by non-linear

9   transfer block 168.   Non-linear transfer block 168 is preferably configured to produce an

10   output signal which is a function of input signals noise threshold 158 and noise reduction

11   level 30 which has a transfer characteristic as shown in the graph of FIG. 7. The inputs

12   158 and 30 select an operating curve above which detected motion will not permit noise

13   reduction, in order to prevent motion artifacts. As will be appreciated by those of ordinary

14   skill in the art, non-linear transfer block 168 may be configured from a ROM lookup table.

15   An example of a suitable ROM lookup table is provided in Appendix I.

16   The output of multiplier 166 is presented to one input of adder 170. The output of

17   adder 170 forms the video output of the recursive filter. It also serves as a feedback point

18   and is connected to frame delay 172, which introduces a delay of one frame. The output of

19   frame delay 170 is presented to the other input of subtractor 160, as well as to the input of

20   delay 174, which matches the delay produced by delay 164.   Other than the function of non-

21   linear transfer block 168, the operation of recursive filter 14 is disclosed in United States

22   Patent No. 4,058,836.

23   A set of schematic diagrams for the circuitry which implements an actual

24   embodiment of the invention is filed herewith as Appendix I.   Specifications for the

25   programmable devices shown thereon, is filed herewith as Appendix II. The program-

26   control source code for an Intel 8031 microcontroller which accepts the user commands and

27   interfaces to the system bus of the actual embodiment of the present invention described in

12

1 Appendices I and II is filed herewith as Appendix III. These diagrams and other information,

2 which describe an actual working embodiment of the present invention, are expressly

3 incorporated herein by reference.

4   Those of ordinary skill in the art will recognize that the settings for the various

5 threshold values specified herein are somewhat subjective. The possibilities of

6 combinations of dirt, noise, and motion in video sequences are virtually infinite and thus the

7 threshold settings at any moment may depend on the particular video material being viewed.

8   While embodiments and applications of this invention have been shown and described,

9 it would be apparent to those skilled in the art that many more modifications than mentioned

1 0 above are possible without departing from the inventive concepts herein. The invention,

1 1 therefore, is not to be restricted except in the spirit of the appended claims.

1   <u>What is Claimed is:</u>

2   1.   Apparatus for enhancement of digital video images, said apparatus connectable

3   to a source of digital video signals operating at a video pixel rate and comprising:

4   a median filter including storage means for temporarily storing digital data to

5   present simultaneously data representing pixels from a current video frame, a most recent

6   video frame, and a next video frame;

7   user-selectable data cluster selection means associated with said median

8   filter and operating on each pixel in said current video frame, for identifying one of a

9   plurality of clusters of digital data as a selected cluster from digital data stored in one or

10   more of said current video frame, said most recent video frame, and said next video frame,

11   each of said clusters comprising digital data representing said each pixel and ones of said

12   pixels which are chosen from positional and temporal neighbors of the one of said each

13   pixels being operated on, wherein at least one of said digital data may be weighted more than

14   once, and for presenting said clusters of digital data to said median filter;

15   motion detector means for detecting motion in a region of said current video

16   frame containing said each pixel, and for producing a motion-sense signal proportional to

17   the degree of motion in said region, and

18   first substitution means for substituting an output of said median filter for

19   said each pixel in said current video frame only if said motion-sense signal is below a user-

20   selected threshold.

21

22   2.   The apparatus of claim 1, further including:

23   first means for generating, for each pixel, a deviation threshold signal if said

24   each pixel deviates from the median value of said selected cluster by at least a selected

25   threshold, said selected threshold being adjustable by a user;

26   second substitution means for substituting an output of said median filter for

27   said each pixel in said current video frame in response to said deviation threshold signal.

1

2   3.   The apparatus of claim 1, wherein said plurality of clusters are chosen from

3   the group including:

4   (1)   said each pixel weighted twice, its upper and lower nearest neighbors,

5   each weighted once, and its corresponding pixels in said most recent video frame and said

6   next video frame, each weighted twice;

7   (2)   said each pixel weighted twice, its left and right nearest neighbors,

8   each weighted once, and its corresponding pixels in said most recent video frame and said

9   next video frame, each weighted twice;

1 0   (3)   said each pixel weighted twice, its upper, lower, left, and right

1 1   nearest neighbors, each weighted once, and its corresponding pixels in said most recent

1 2   video frame and said next video frame, each weighted twice;

1 3   (4)   said each pixel weighted twice, its four diagonal nearest neighbors,

1 4   each weighted once, and its corresponding pixels in said most recent video frame and said

1 5   next video frame, each weighted twice;

1 6   (5)   said each pixel weighted twice, its upper, lower, left, and right

1 7   nearest neighbors, each weighted once, its corresponding pixels in said most recent video

1 8   frame and said next video frame, each weighted twice, and their left and right nearest

1 9   neighbors, each weighted once.

2 0

2 1   4.   The apparatus of claim 1, further including a recursive filter having an

2 2   input connected to said output of said median filter.

2 3

2 4   5.   The apparatus of claim 4, wherein said recursive filter includes:

2 5   noise threshold setting means;

2 6   noise reduction level control means;

2 7   motion detector means for detecting motion in a region of said current video

15

1   frame containing said each pixel, and for producing a motion-sense signal proportional to

2   the degree of motion in said region; and

3   recursion control means, responsive to said motion-sense signal, said noise

4   ' threshold setting means, and said noise reduction level control means, for controlling the

5   magnitude of recursion produced by said filter.
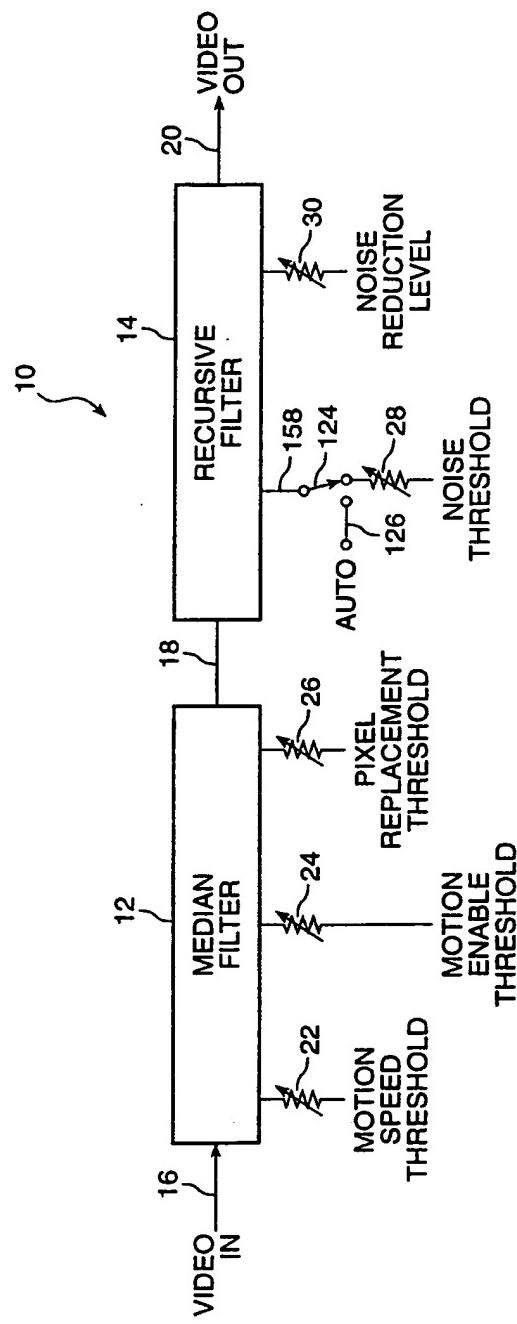
FIG. 1
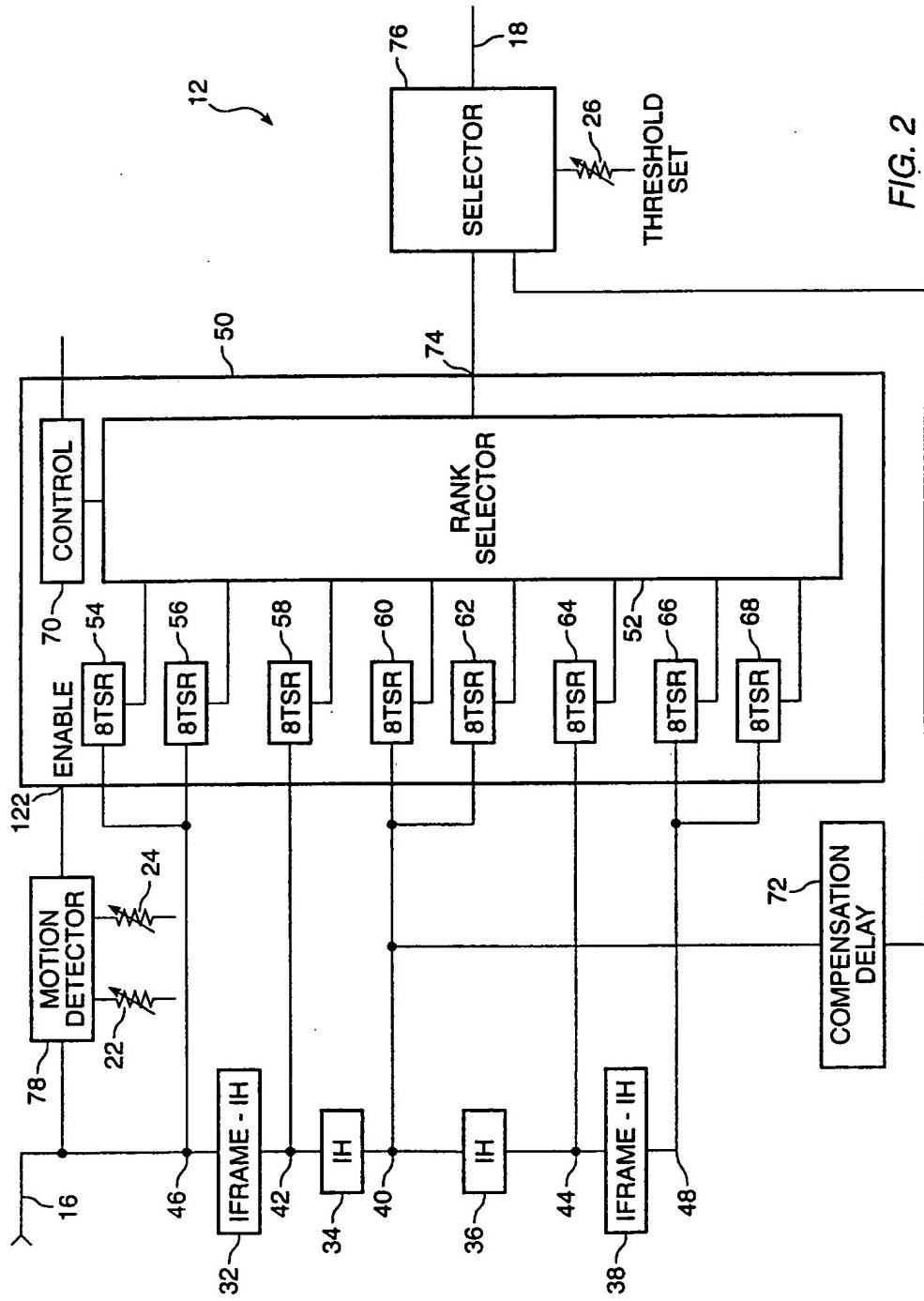
FIG. 2
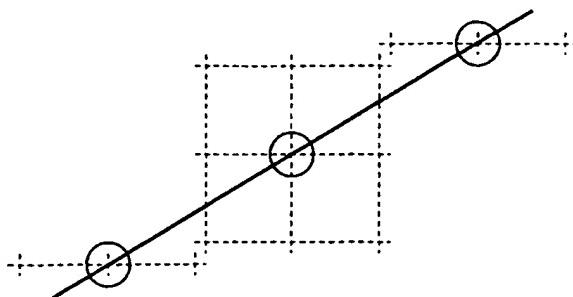
FIG. 3a
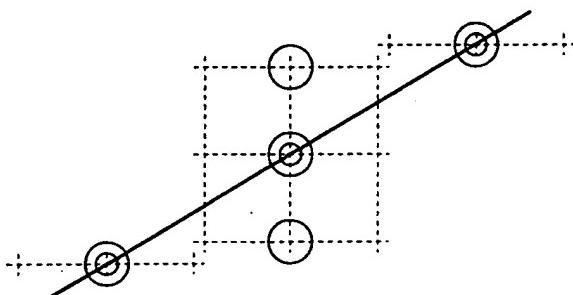
FIG. 3b
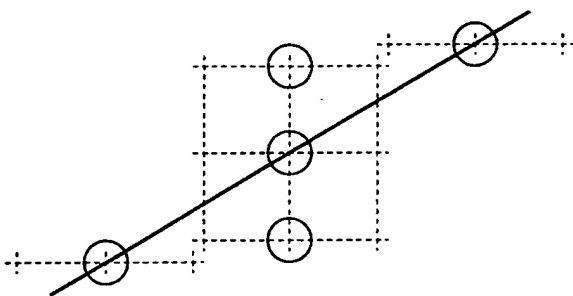
FIG. 3c
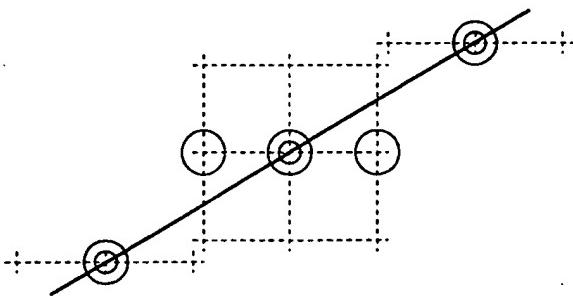


FIG. 3d
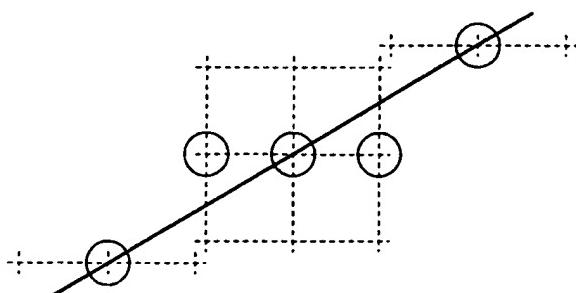
FIG. 3e
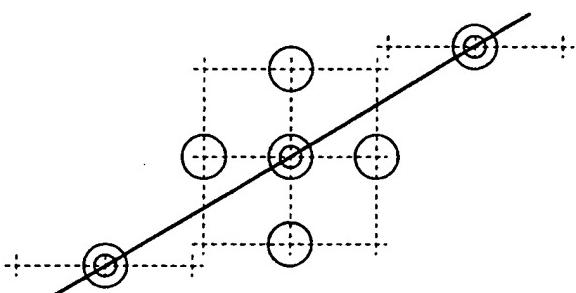
FIG. 3f
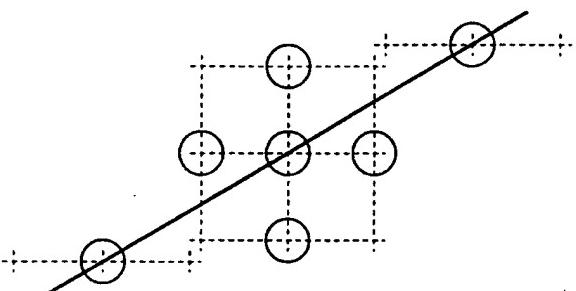
FIG. 3g
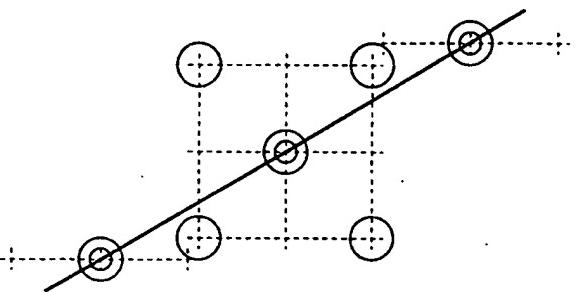
FIG. 3h
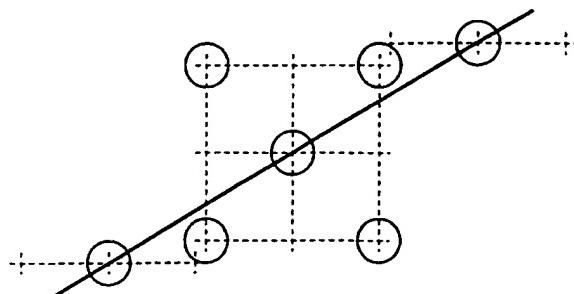
FIG. 3i

FIG. 3j

FIG. 3k

FIG. 3l

5 / 8
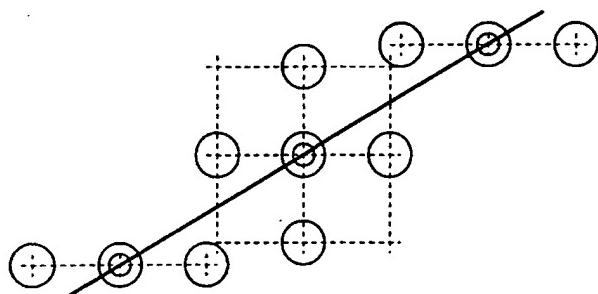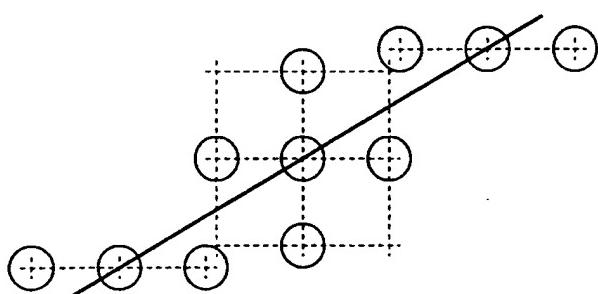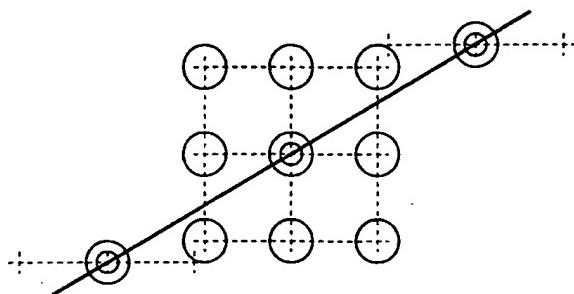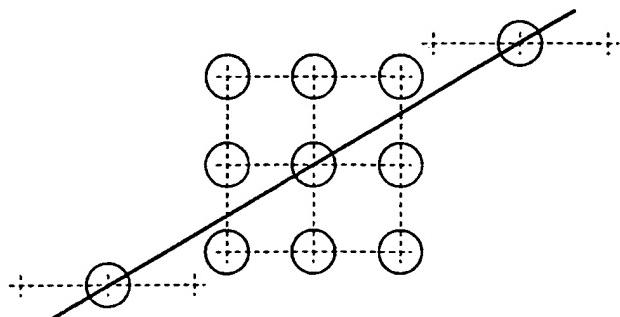
FIG. 3m
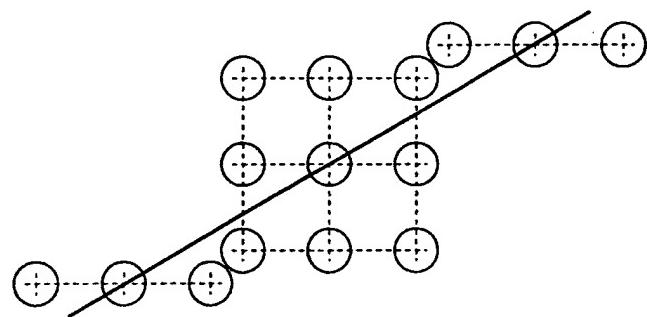
FIG. 3n
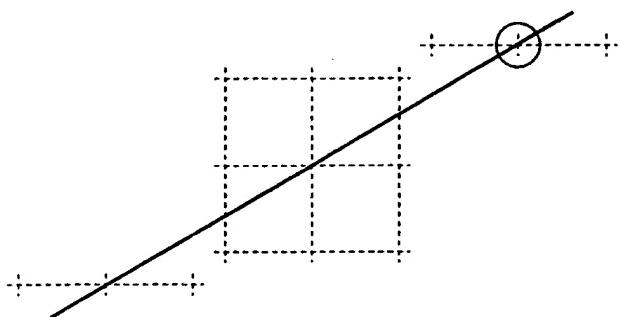
FIG. 3o

FIG. 4
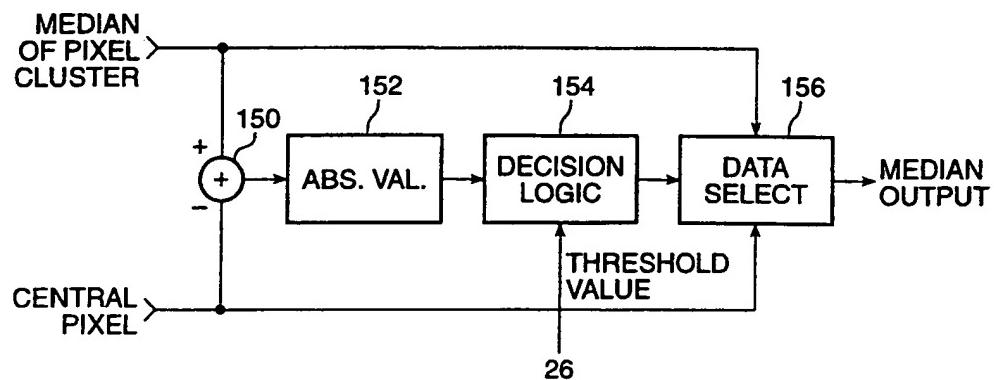
FIG. 5
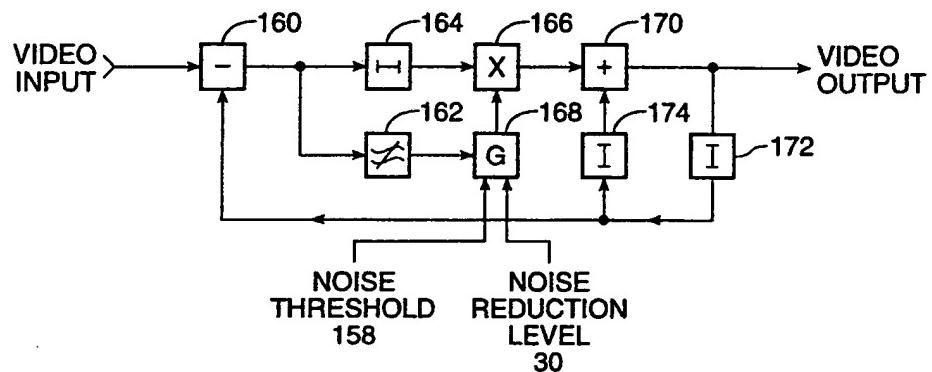
FIG. 6
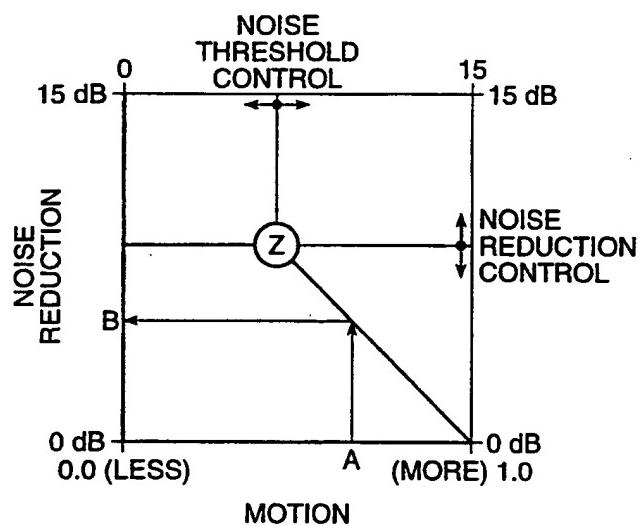
FIG. 7

8 / 8

A.	CLASSIFICATION OF SUBJECT MATTER

IPC(5)   :H04N 5/213
US CL   :358/167, 166, 105

According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. :   358/167, 166, 105; H04N 5/213

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C.	DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB, A, 2 251 353 (BORER) 26 September 1988, figure 1, abstract	1
A	GB, A, 2 202 706 (WISCHERMANN) 01 July 1992, figure 3, abstract	1
A	US, A, 4,682,230 (PERLMAN ET AL.) 21 July 1987, figures 3 & 4	1
A,P	US,A, 5,161,018 (MATSUNAGA) 03 November 1992, figure 1	1,5
A	US, A, 4,928,258 (MAY) 22 May 1990, figure 16	1
A	US, A, 5,068,914 (KLEES) 26 November 1991, abstract, figure 3	3

X	Further documents are listed in the continuation of Box C.		See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 January 1994	MAR 14 1994

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Jeffrey S. Murrell
Facsimile No. NOT APPLICABLE	Telephone No. (703) 305-8155

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,058,836 (DEWERY ET. AL.) 15 November 1977, abstract, figure 3.	1-5